27128A
128K (16K x 8) PRODUCTION AND UV ERASABLE PROMs

- **Fast 150 nsec Access Time**
  — HMOS* II-E Technology
- **Low Power**
  — 100 mA Maximum Active
  — 40 mA Maximum Standby
- **int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **± 10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec, Order #231369)

The Intel 27128A is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128A is fabricated with Intel's HMOS* II-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

The 27128A is currently available in the CERDIP package providing flexibility in prototyping and R&D environments where reprogrammability is required.

The 27128A is available in fast access times including 150 ns (27128A-1). This ensures compatibility with high-performance microprocessors, such as Intel's 8 MHz 80186 allowing full speed operation without the addition of WAIT states. The 27128A is also directly compatible with the 12 MHz 8051 family.

*HMOS is a patented process of Intel Corporation.

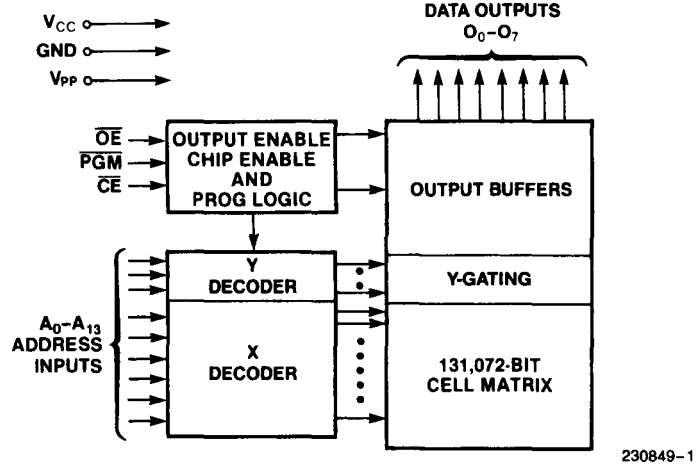


Figure 1. Block Diagram

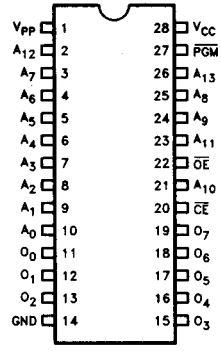
October 1990
Order Number: 230849-009

Pin Names

A_0-A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

27512 27C512	27256 27C256	2764A 27C64 87C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27128A



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2716	2732A	2764A 27C64 87C64	27256 27C256	27512 27C512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128A Pins

Figure 2. Cerdip(D) DIP Pin Configuration

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EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27128A Versions

Packaging Options	
Speed Versions	**Cerdip**
-20	T, L, Q

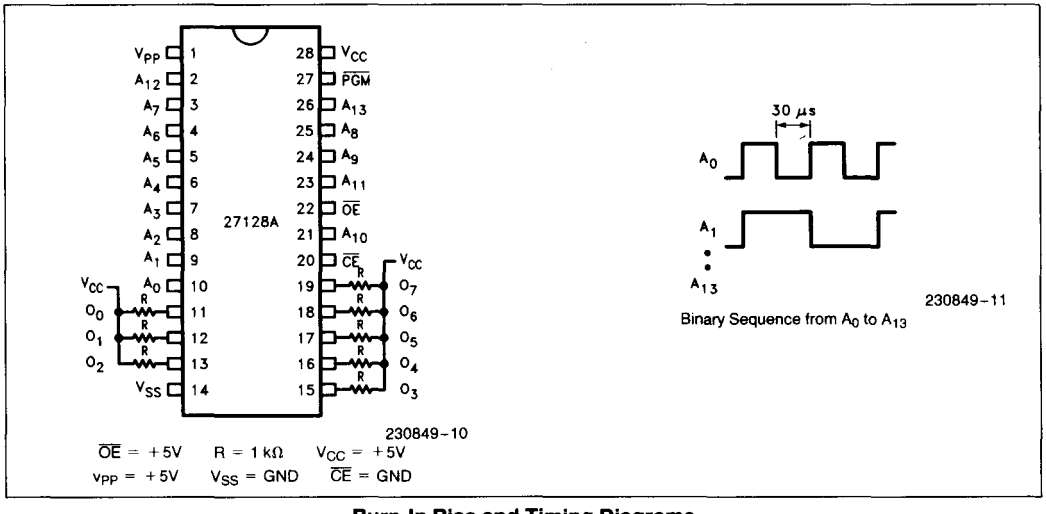
READ OPERATION

DC CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27128A, LD27128A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with Outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.25V
Voltage on A_9 with Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Notes	Limits			Units	Conditions
			Min	Typ(3)	Max		
I_{LI}	Input Load Current				10	µA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current				10	µA	$V_{OUT} = 0V$ to V_{CC}
I_{PP1}	V_{PP} Current Read	2			5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby				40	mA	$\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Current Active	2			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		+0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -400$ µA
V_{PP}	V_{PP} Read Voltage	2	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25$

AC CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(5)	$V_{CC} \pm 5\%$	Notes	27128A-1		27128A-2		27128A		Unit
	$V_{CC} \pm 10\%$				27128A-20		27128A-25		
Symbol	Characteristics		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay			150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay			65		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	4	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	4	0		0		0		ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

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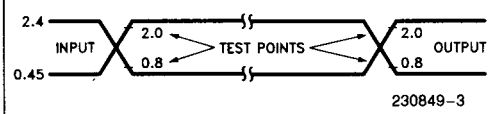
CAPACITANCE[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

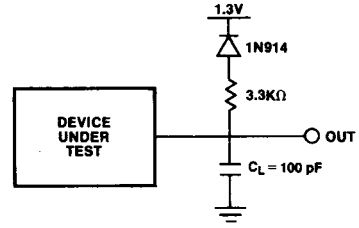
AC TESTING INPUT/OUTPUT WAVEFORM



230849-3

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

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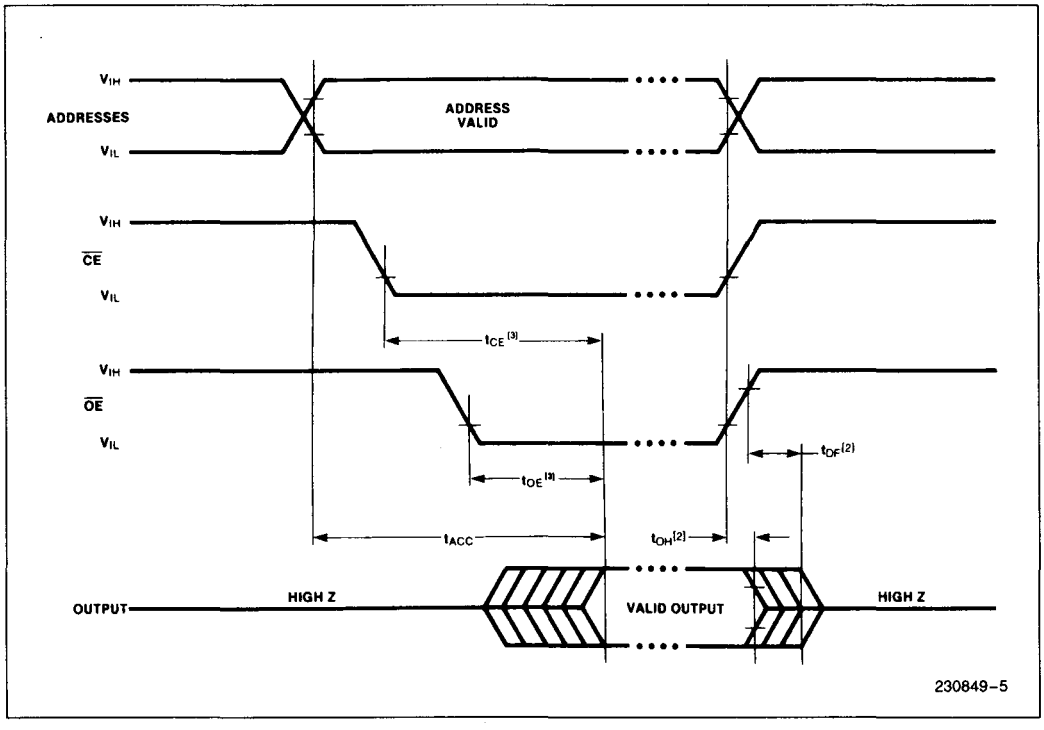
AC WAVEFORMS



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NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	D_{OUT}
Output Disable			V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		4	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.0V	D_{IN}
Program Verify		4	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.0V	D_{OUT}
Program Inhibit		4	V_{IH}	X	X	X	X	V_{PP}	6.0V	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{CC}	5.0V	89 H
	Device	2, 3	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	5.0V	89 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1-A_8, A_{10}-$A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27128A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

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PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

inteligent Identifier Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

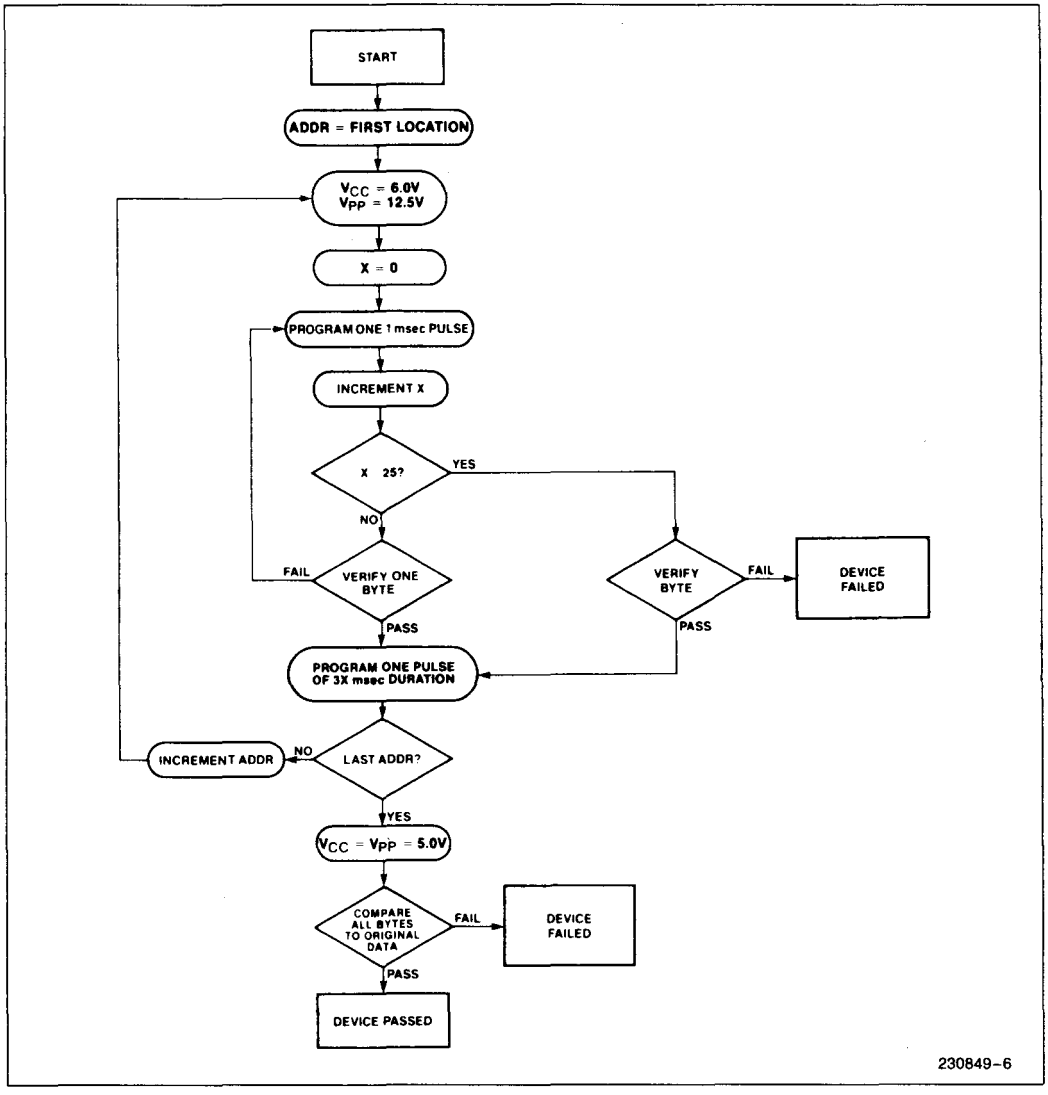

Figure 3. int$_e$ligent Programming Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming™ Algorithm, a standard in the industry for the past few years, is required for the 27128A. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 3.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

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DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	intelligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	intelligent Programming Algorithm	5.75	6.25	V	

AC PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

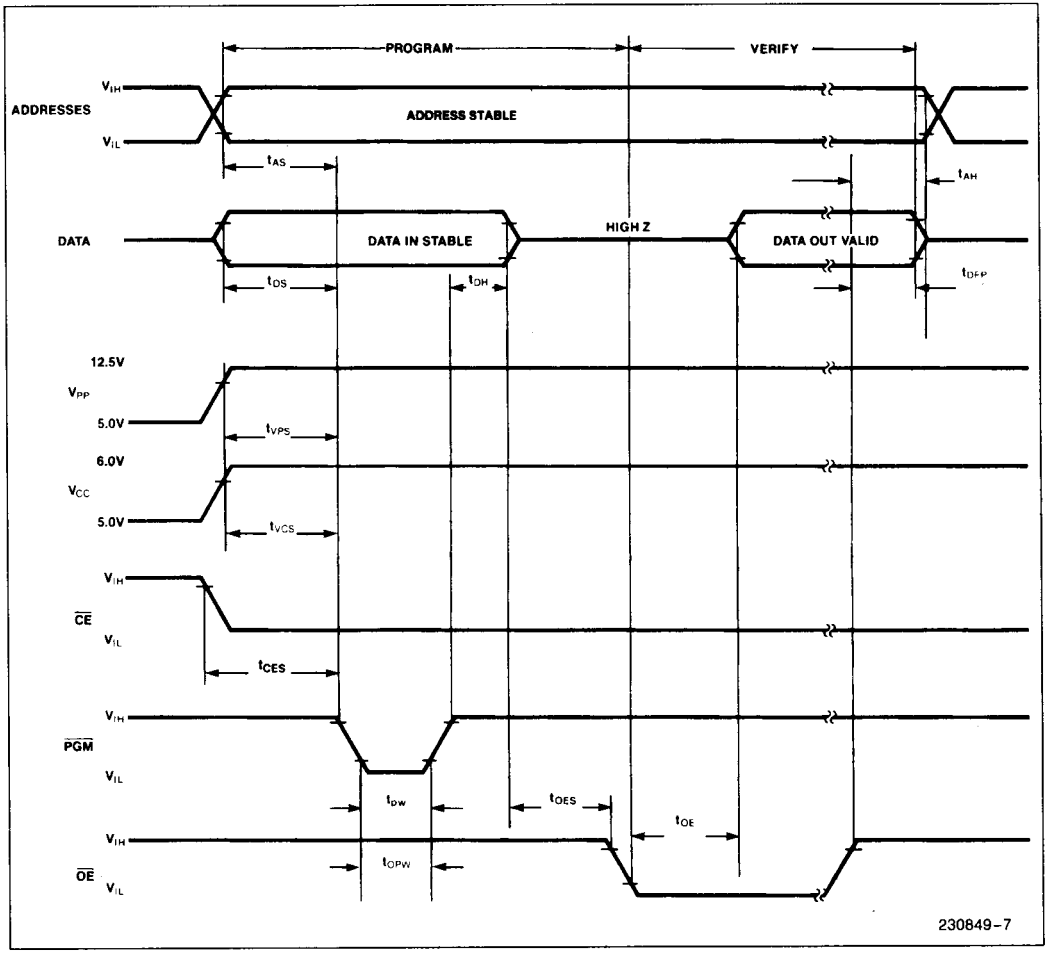
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

REVISION HISTORY

Number	Description
009	Removed Plastic Package